REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action dated May 3, 2005 (hereinafter the Official Action). In response, Applicants respectfully traverse the rejection of Claims 1 – 13 as the basis provided in the Official Action does not meet the requirements of a rejection under § 102 for at least the reasons discussed herein. Accordingly, Applicants respectfully request the withdrawal of the rejections and the allowance of all claims.

Independent Claim 1 is patentable over Ballantine.

Claims 1 – 13 stand rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,444,592 to Ballantine et al. ("Ballantine"). *Official Action*, page 2. As briefly discussed above, Applicants respectfully traverse the rejection as a basis provided in the Official Action does not meet the stringent requirements of a rejection under § 102. Respectfully, anticipation under § 102 requires that each and every element of the claim is found in a single prior art reference. *W. L. Gore & Associates Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Stated another way, all material elements of a claim must be found in one prior art source. *In re Marshall*, 198 U.S.P.Q. 344 (C.C.P.A 1978). "Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention." *Apple Computer Inc. v. Articulate Systems Inc.* 57 USPQ2d 1057, 1061 (Fed. Cir. 2000). A finding of anticipation further requires that there must be no difference between the claimed invention and the disclosure of the cited reference as viewed by one of ordinary skill in the art. *See Scripps Clinic & Research Foundation v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). Additionally, the cited prior art reference must be enabling, thereby placing the allegedly disclosed matter in the possession of the public. *In re Brown*, 329 F.2d 1006, 1011, 141 U.S.P.Q. 245, 249 (C.C.P.A. 1964). Thus, the prior art reference must adequately describe the claimed invention so that a person of ordinary skill in the art could make and use the invention.

Independent Claim 1 recites in part:

> **nitriding** a high dielectric layer on a silicon substrate, **wherein said high dielectric layer comprises a nano laminate comprising a Group 3 metal oxide layer and a layer selected from the group consisting of a hafnium oxide layer and a zirconium oxide layer and wherein an ozone oxide layer is positioned between said high dielectric layer and said silicon substrate**; and
> post treating the high dielectric layer, ozone oxide layer, and silicon substrate.

Applicants respectfully submit that Ballantine does not does not disclose at least the above highlighted recitations of independent Claim 1. In particular, the cited passage of Ballantine (alleged to meet the above emphasized recitations of independent Claim 1) appears to discuss forming the interfacial layer 14 using a rapid thermal anneal, oxynitridation or nitradation. In other words, it appears that Ballantine actually uses nitriding to form what the Official Action alleges is the ozone oxide layer recited in independent Claim 1. In contrast, independent Claim 1 recites nitriding the high dielectric layer including the nano laminate (*i.e.* the Group 3 metal oxide layer and layer selected from the group consisting of hafnium oxide and zirconium oxide) as well as the ozone oxide layer. Accordingly, Ballantine does not disclose the recitations of Claim 1 as any nitriding performed by Ballantine is complete once the interfacial layer 14 is formed. Therefore, according to Ballantine, the high dielectric layer is formed **after** nitriding.

Accordingly, Applicants respectfully submit that independent Claim 1 is patentable over Ballantine for at least these reasons. Furthermore, dependent Claims 2 – 13 are also patentable over Ballantine for at least the reasons discussed above in reference to independent Claim 1.

In addition to the above reasons, Applicants respectfully submit that Ballantine also does not disclose (in accordance with the stringent requirements of § 102) at least "nitriding ... an ozone oxide layer." The Official Action appears to assert that the above highlighted recitations of independent Claim 1 are met by element 14 in Figure 1 and column 3, lines 58 – 65 and column 8 lines 45 – 50 of Ballantine. Column 3, lines 59 – 67 of Ballantine reads:

> Next, ultra-thin interfacial oxide, oxynitride and/or nitride layer 14 is formed on the substrate utilizing one of the processing techniques that will be mentioned hereinbelow in more detail. The ultra-thin interfacial oxide, oxynitride and/or nitride layer of the present invention has a thickness of less than about

> 10A, with a thickness of from about 2 to 8 .ANG. being more highly preferred. The present invention also contemplates mixtures or multilayers of said oxide, oxynitride or nitride. *Ballantine*, column 3, lines 59 – 67.

As understood by Applicants, the Official Action appears to consider discussion of the ultra thin interfacial oxide to disclose the ozone oxide layer recited in independent Claim 1. However, Applicants respectfully submit that an oxide layer does not disclose an ozone oxide layer. Furthermore, the methods discussed in Ballantine for the formation of the oxide layer also do not disclose the formation of an ozone oxide layer (in compliance with the strict requirements of § 102. In particular, Ballantine, column 8, lines 45 – 50 recite:

> 16. The method of claim 15 wherein said plasma oxidation process includes O.sub.2 plasma immersion of Si wafers for about 5 to about 300 seconds.
>
> 17. The method of claim 14 wherein said oxide is formed by an ozone process.
>
> 18. The method of claim 14 wherein said oxide is formed by a low-energy oxygen implantation process and a rapid thermal anneal process.

Applicants respectfully submit that the above recitations in Ballantine do not disclose an ozone oxide layer. Similarly, the portion of the specification that appears to discuss the ozone process recited in Claim 17 recites:

> Another technique that can be employed in the present invention in forming the ultra-thin interfacial layer is by **using an ozone process in which ozone is used to grow an ultra-thin interfacial layer**. The ozone process may be carried out using the RTO temperatures or times mentioned above or conventional furnace conditions which include much longer heating times may be used. *Ballantine*, column 6, lines 66 & 67, column 7, lines 1 – 5. Emphasis added.

As understood by Applicants, the above-cited passage of Ballantine demonstrates that the only discussion therein is a generic ozone process used to grow an ultra thin interfacial layer that does not disclose or suggest formation of an ozone oxide layer. In contrast, the interfacial layer 11 is discussed in detail in Applicants disclosure, for example, in paragraph 36:

> According to other embodiments of the present invention, the high dielectric layers 12 may be formed over an interfacial layer 11. The interfacial layer 11 may include an ozone oxide layer deposited over a silicon substrate or

integrated circuit on which a high dielectric layer 12 is to be formed. An ozone oxide interfacial layer 11 may be formed on a silicon substrate 10 using ozone. For example, an ozone oxide interfacial layer 11 may be deposited on a silicon substrate 10 by flushing the silicon substrate 10 with ozone *in situ*. In other embodiments, an ozone oxide interfacial layer 11 may be applied with an atom layer depositing device similar to those used to form a high dielectric layer 12. In other embodiments the ozone oxide interfacial layer 11 may be formed using a chemical evaporation depositing device or chemical vapor deposition. In some embodiments, the ozone oxide interfacial layer 11 is formed with a thickness of about 8 Å or less. The ozone oxide interfacial layer 11 may also be formed at a temperature of between about 320 ^{O}C to about 450 ^{O}C. The presence of an ozone oxide interfacial layer 11 between a high dielectric layer 12 and a substrate can reduce the leakage current negative bias temperature instability (NBTI) of the device. The interfacial layer 11 may be formed prior to the deposition of the nano laminate that forms the high dielectric layer 12.

Accordingly, Applicants respectfully submit that independent Claim 1 is patentable over Ballantine for at least these additional reasons

New Claim 46 is patentable.

Applicants have added new independent Claim 46, which recites in part:

> nitriding a high dielectric layer on a silicon substrate, wherein said high dielectric layer comprises a multi-layered nano laminate formed by forming a hafnium oxide layer or a zirconium oxide layer on the substrate using atomic layer deposition and then forming a Group 3 metal oxide layer thereon using atomic layer deposition, wherein an ozone oxide layer is positioned between the high dielectric layer and the silicon substrate; and
>
> post treating the high dielectric layer and silicon substrate.

Applicants submit that new Claim 46 is patentable for at least the reasons discussed herein above.

CONCLUSION

Applicants have shown that Claims 1 – 13 are patentable over Ballantine. Accordingly, Applicants respectfully request the withdrawal of all rejections and the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

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